REMARKS

Claims 1-15 are pending. By this amendment, claims 5, 7, and 11 are amended. No new matter is introduced. Reconsideration and allowance of the claims in view of the above amendments and the remarks that follow are respectfully requested.

Claim Objections

On page 2 the Office Action objects to claims 5, 11, and 13 as being informal. These claims have been amended as suggested by the Office Action. Withdrawal of the objections to claims 5, 11, and 13 is respectfully requested.

Rejections for Non-Statutory Obviousness-Type Double Patenting

On page 2 the Office Action rejects claims 1-15 for non-statutory obviousness-type double patenting. Applicants are filing herewith a terminal disclaimer as to claims 1-15. Withdrawal of the rejection of claims 1-15 for non-statutory obviousness-type double patenting is respectfully requested.

Rejections under 35 U.S.C. § 103(a)

Claims 11, 12, and 14. Claims 11, 12 and 14 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 5,732,235 to Kahle (hereafter Kahle) in view of U.S. Patent 5,537,559 to Kane et al. (hereafter Kane). Applicants respectfully traverse each of these rejections.

To establish a *prima facie* case of obviousness, the prior art references must teach or suggest all the claim limitations. MPEP § 2143; e.g., In re Royka, 490 F.2d 981, 985 (CCPA 1974) (holding that establishing a prima facie obviousness requires that all the claim limitations must be taught or suggested by the prior art). Kahle and Kane disclose neither a "fetch complete signal" nor a "fetch address queue [that] is controlled by the fetch complete signal," as specified in claim 11.

As acknowledged by the Examiner, Kahle does not describe the following limitations of claim 11: (i) that an engine of the emulated ISA receives a fetch complete signal from the fetch engine; or (ii) a fetch address queue that stores a fetch address for the line of instructions retrieved from the memory subsystem, wherein the fetch address queue is controlled by the fetch complete signal such that the fetch address is stored in the fetch address queue until the fetch complete signal is received. (Office action at 12-13). The

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Examiner finds such teachings in Kane: the Examiner finds that the "fetch-exception status bits" shown in Kane (Fig. 4, component 480; Col. 11, ll. 13-22; Col. 11, ll. 59 - Col. 12, ll. 3) meet the limitation of the "fetch complete signal" of claim 11, that the fetch address queue of Kane (Fig. 4, component 400) meets the limitation of the "fetch address queue" of claim 11 (Office action at 12-13), and that it would have been obvious to a person of ordinary skill to combine the two references. (Office action at 12-14).

Applicants respectfully disagree. Kane nowhere identifies or describes a "fetch complete" signal or a signal that signifies that a fetch has been completed. The "fetch-exception status bits" convey data regarding what *kind* of exception is associated with each instruction byte, i.e., either a limit error, page fault, breakpoint, or no exception. (Kane, Col. 11, ll. 16-22; Col. 12, ll. 1-3; Fig. 1; Col. 6, ll. 27-48). However, Kane neither states nor implies that the fetch-exception status bits signify "fetch complete." Indeed, the state of the fetch exception status bits in Kane is *independent* of the completion status of the fetch request, since the fetch request status bits for each fetch request are stored as data in the fetch address queue along with the corresponding fetch address until the fetch request is completed. (Kane, Col. 11, ll. 13-16; Col. 12, ll. 12-13). Although (as noted by the Examiner) the fetch status bits are provided simultaneously with the fetch data to the instruction buffer (Kane, Col. 11, ll. 64-67), Kane nowhere describes the fetch-exception status bits as "controlling" the fetch address queue.

Further, to establish a *prima facie* case of obviousness, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. MPEP § 2143; In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). No suggestion or motivation is found in Kane or Kahle to combine the exception status bits or fetch address queue of Kane with the method and system shown in Kahle. The Examiner finds such motivation because a person of ordinary skill (i) would have recognized that the exception signals of Kane "would be applicable in Kahle's system since Kahle is concerned with address exceptions," and (ii) would have modified Kahle "to include a fetch address queue as taught in Kane to store and postpone fetch requests to avoid unnecessary suspension of the CPU." (Office action, at 12-13). Neither of these issues, however, is part of the problem addressed by Kahle. Kahle is concerned with reducing the cycle time required to process a sequence of emulated instructions, and it solves the problem by eliminating the need for a separate fetch request to

decode a branch instruction in some instances. (Kahle, Col. 1, ll. 14 to Col. 2, ll. 4; Col. 4, ll. 28-40). Kahle expresses no concern regarding delays in fetching the instructions caused by incomplete fetches or bus suspensions.

In summary, claim 11 is not rendered obvious by Kahle in light of Kane. Neither Kahle nor Kane specify the fetch complete signal or the fetch address queue controlled by the fetch complete signal of claim 11, and there is no motivation or suggestion to combine the references. Reconsideration of the rejection of claim 11 is requested.

The Examiner rejected claims 12 and 14 as obvious in light of Kahle and Kane. Claims 12 and 14 depend from claim 11. Because claim 11 is not obvious over Kahle and Kane, claims 12 and 14 are likewise not obvious over Kahle and Kane. In re Fine, 837 F.2d 1071, 1076 (Fed. Cir. 1988) (dependent claims are nonobvious under section 103 if the independent claims from which they depend are nonobvious). Reconsideration of the rejection of claims 12 and 14 is requested.

Claim 13. Claim 13 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Kahle in view of Kane and further in view of U.S. Patent 5,515,521 to Whitted et al. (hereafter Whitted). Applicant respectfully traverses the rejection. Claim 13 depends from claim 11. As discussed above with respect to claim 11, the combination of Kahle, Kane, and Whitted does not show the fetch complete signal or the fetch address queue controlled by the fetch complete signal of claim 11. Because claim 11 is not obvious over Kahle, Kane, and Whitted, claim 13 is likewise not obvious over Kahle, Kane, and Whitted. In re Fine, 837 F.2d 1071, 1076. Reconsideration of claim 13 is requested.

Claim 15. Claim 15 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Kahle in view of Kane and further in view of U.S. Patent 5,584,037 to Papworth et al. (hereafter Papworth). Applicant respectfully traverses the rejection. Claim 15 depends from claim 14. As discussed above with respect to claims 11 and 14, the combination of Kahle and Kane does not show the fetch complete signal or the fetch address queue controlled by the fetch complete signal of claim 11. Papworth likewise does not show the fetch complete signal or the fetch address queue controlled by the fetch complete signal of claim 11. Thus claim 11 is not obvious over Kahle, Kane, and Papworth. Claim 14, which depends from claim 11, therefore is not obvious over Kahle, Kane, and Papworth. In re Fine, 837 F.2d 1071, 1076. Claim 15, which depends from claim 14, likewise is not obvious over Kahle, Kane, and Papworth. Id. Reconsideration of the rejection of claim 15 is requested.
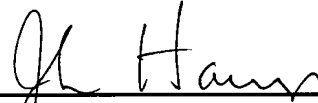
Conclusion

The Office Action contains a number of statements potentially reflecting characterizations of various claims, supporting descriptions, and/or patent or patent application references. Regardless of whether any such statements are addressed in this response, Applicants decline to automatically subscribe to any statement or characterization in the Office Action. Although the Examiner's rejection of claims 1-15 has been completely traversed as set forth above without reference to many of such statements, Applicants hereby expressly reserve the right to dispute such statements later.

In view of the reasons given above, Applicants respectfully request reconsideration of the pending application, withdrawal of all the claim rejections and objections, and the timely allowance of claims 1-15.

Should the Examiner believe that anything further is desired in order to place the application in even better condition for allowance, the Examiner is invited to contact Applicants' undersigned representative at the telephone number listed below.

Respectfully submitted,

Date: **September 19, 2006**

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Attachment: Terminal Disclaimer

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